Amendments to the Drawings:

The attached replacement sheets of drawings includes changes to Figs. 2-2, 3 and 5, and replace the original sheets including Figs 2-2, 3 and 5.

In Figure 2-1, applicant changed the reference numeral 14, pointing to the multithreaded processor shown in the figure, to reference numeral 12. Applicant further removed reference numeral 56 which was pointing to the element block identified as "PLL GRAMMAR."

In Figure 2-2, applicant changed the reference numeral 29, pointing to the element block identified as the Scratch Pad, to reference numeral 27. Further, applicant replaced "SDRAM" with "SRAM" in element block 16b.

In Figure 3, the applicant marked the element identified as uPC_1 with reference numeral 72a (which previously pointed to uPC_4), uPC_2 with reference numeral 72b (which previously pointed to uPC-1), and uPC_3 with reference numeral 72c (which previously pointed to the illustrated multiplexer). Additionally, applicant added new reference numeral 72d to mark uPC_4.

In Figure 5, applicant changed the notation "Srl" to "Src" and changed the notations of "1" to "1".

Attachments following last page of this Amendment:

Annotated Sheet Showing Change(s) (4 pages)

Replacement Sheet (6 pages)

REMARKS

Applicant thanks the examiner for his help in resolving the outstanding issues in relation to the previously submitted Information Disclosure Statements.

In response to the Notice of Allowability, dated August 23, 2006, applicant submits herewith a complete set of formal drawings. Applicant has amended Figs. 2-1, 2-2, 3 and 5 to correct typographical errors, to promote clarity, and to make the drawings consistent with the written description.

Please apply any required fees to deposit account 06-1050, referencing the attorney docket number shown above.

Respectfully submitted,

Date: November 17, 2006

Ido Rabinovitch
Reg. No. L0080

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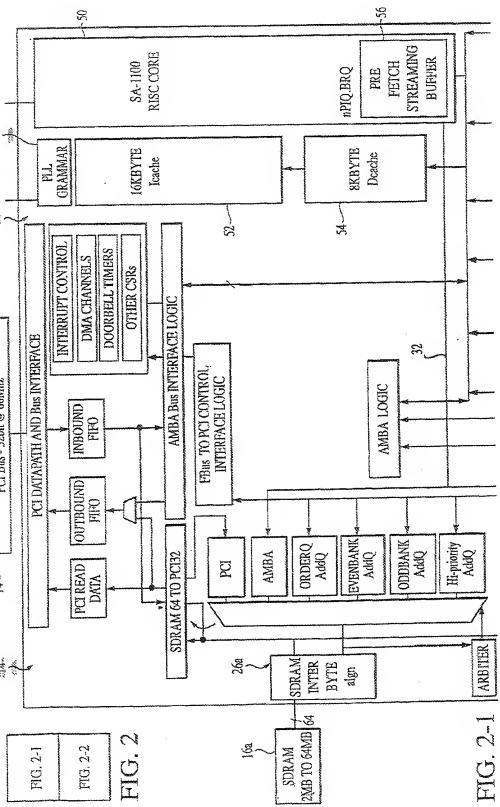


FIG. 2-1

FIG. 2-2

FIG. 2

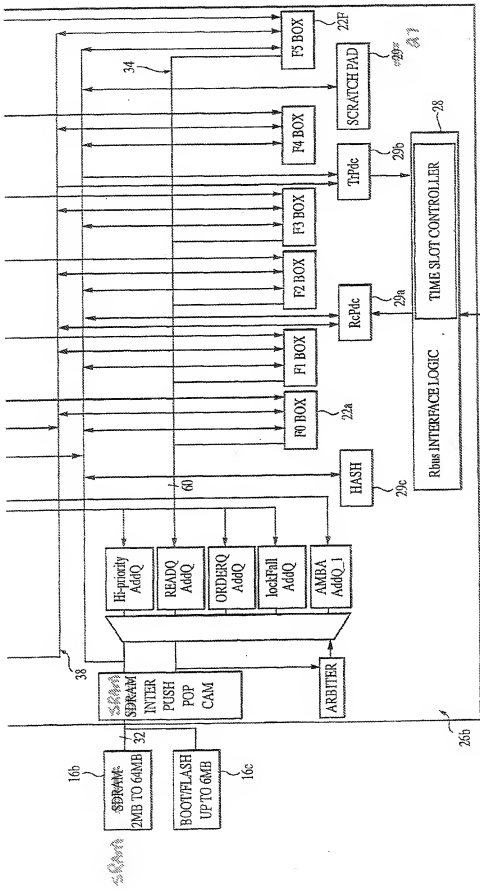

F5 BOX
22f
SCRATCH PAD
29e
34
F4 BOX
TPdc
29b
28
F3 BOX
F2 BOX
RcPdc
29a
TIME SLOT CONTROLLER
F1 BOX
F0 BOX
22a
HASH
29c
Rbus INTERFACE LOGIC
F Bus - 64bit @ 66Mhz
18
60
Hi-priority AddQ
READQ AddQ
ORDERQ AddQ
lockFail AddQ
AMBA AddQ_1
38
SDRAM INTER PUSH POP CAM
ARBITER
32
26b
16b
SDRAM 2MB TO 64MB
BOOTFLASH UP TO 6MB
16c

FIG. 2-2

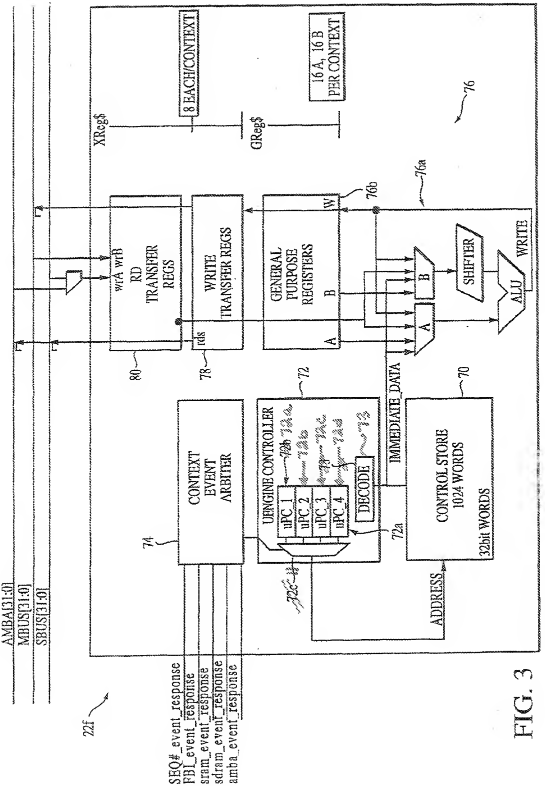
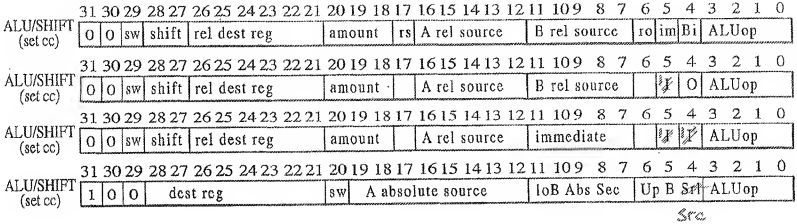

AMBA[31:0]
MBUS[31:0]
SBUS[31:0]
XReg$
8 EACH/CONTEXT
GReg$
16 A, 16 B PER CONTEXT
76
76a
76b
wrA wrB
RD TRANSFER REGS
WRITE TRANSFER REGS
GENERAL PURPOSE REGISTERS
W
B
A
rds
80
78
SHIFTER
ALU
WRITE
IMMEDIATE_DATA
72
70
CONTEXT EVENT ARBITER
UENGINE CONTROLLER
uPC_1
uPC_2
uPC_3
uPC_4
DECODE
72a
74
CONTROL STORE 1024 WORDS
32bit WORDS
ADDRESS
22f
SEQ#_event_response
FBI_event_response
sram_event_response
sdram_event_response
amba_event_response

FIG. 3



Shift Decode:

(rs,r0) decode ([31:0] shifts into [63:32] and take [63;32]):

00 = left rotate
01 = right shift (32-ShfAmt = Right Shift Amt)
10 = left shift
11= double shift (upper A-op shifts into lower B-op)

===> "left rotate" of zero gives zero shift (therwise zero amount signifies indirect shift)

ALU-OP decode:

0000 = B	0100 = ~A&B (~and)	1000 = A-B	1100 = A+B(8)
0001 = ~B	0101 =XOR	1001 = B-A	1101 = A+B(16)
0010 = A&B (and)	0110 = OR	1010 =	1110 = A+B
0011= A&~B (and~)	0111= mul-stuff	1011=	0011= A+B+Cin

FIG. 5